LS8T41505

V1.2

2024 09

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(Tel) 025-58600707

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	˜	V1.2
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1	V1.0	ṗ
2	V1.03	Δ ΰ
3	V1.04	− Ƕ ₮ ḱ 1
4	V1.1	Ƕ ƀ ί -40 +105 1 Ţ VDDO0 ḱ 1.8V 3.3V XIN ˜ 1.8V 2 Ţ θ J 42 /W 3VDDO0 1.8V Έ 4 Ţ ą PLL ῆ 5 OUTOB β ẅ Ḥ
5	V1.2	ḱ ẅ ṗ Ƕ ESD Ḥ 13 14 36 39 40 ḱ 2 ĩ ḱ 3 ˜ ṿ W ῆ ẅ Ḥ Ţ ḱ LS8T41505 ƀ Ƕ Đ A 245 ; Đ B PCB

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U ⊢ service@loongson.cn

1.

LS8T41505 25MHz LVDS LVCMOS LPHCSL LVCMOS 100MHz LVDS 200MHz LPHCSL 100MHz 4 PC PCIE2.0

2.

- 3.3V 1.8V
- LVCMOS LPHCSL LVDS ‰
-
  - OUT0 25MHz/100MHz LVCMOS
  - OUT1 33.33MHz LVCMOS/100MHz LP-HCSL/25MHz LP-HCSL
  - OUT2 100MHz LVCMOS/100MHz LP-HCSL/200MHz LVDS/156.25MHz LP-HCSL
  - OUT3 5-11 100MHz LP-HCSL
  - OUT4 100MHz/200MHz LVDS/100MHz LP-HCSL
- 25MHz
- -40 +105

3.

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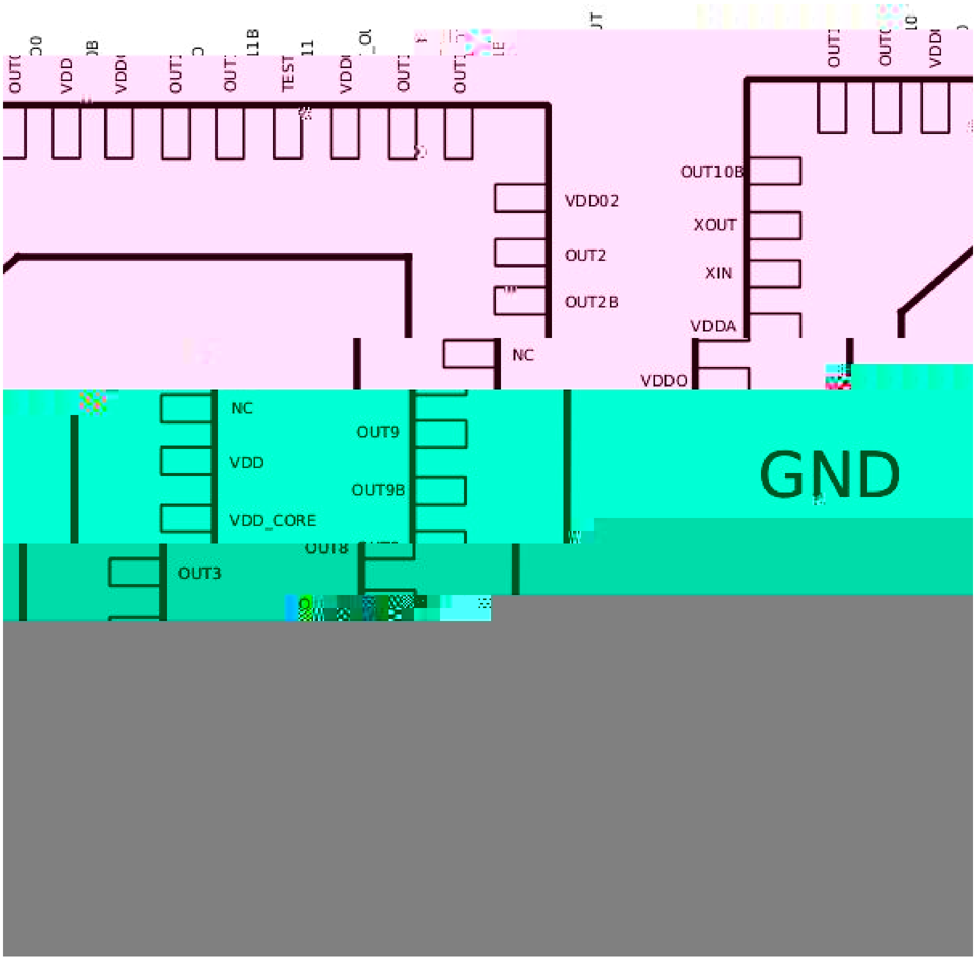

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1	OUT10B	Output	Output Clock10 100MHz LP-HCSL
2	XOUT	Input	
3	XIN/REF	Input	25MHz 25MHz 1.8V
4	VDDA	Power	1.80V
5	VDDO	Power	OUT3 OUT5~11/OUT3B OUT5B~11B 1.80V
6	OUT9	Output	Output Clock9 100MHz LP-HCSL
7	OUT9B	Output	Output Clock9 100MHz LP-HCSL
8	OUT8	Output	Output Clock8 100MHz LP-HCSL
9	OUT8B	Output	Output Clock8 100MHz LP-HCSL
10	OUT7	Output	Output Clock7 100MHz LP-HCSL
11	OUT7B	Output	Output Clock7 100MHz LP-HCSL
12	OE	Input	
13	SEL1	Input	5
14	SEL0	Input	5
15	VDD	Power	1.80V
16	VDDO	Power	OUT3 OUT5~11/OUT3B OUT5B~11B 1.80V
17	OUT6	Output	Output Clock6 100MHz LP-HCSL

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18	OUT6B	Output	Output Clock6 ḭ ₣ 100MHz LP-HCSL Ḥ
19	OUT5	Output	Output Clock5 ₣ 100MHz LP-HCSL Ḥ
20	OUT5B	Output	Output Clock5 ḭ ₣ 100MHz LP-HCSL Ḥ
21	VDDO4	Power	OUT4 3.30V
22	OUT4	Output	Output Clock4 ₣ 100MHz LP-HCSL 100MHz/200MHz LVDS Ḥ
23	OUT4B	Output	Output Clock4 ḭ ₣ 100MHz LP-HCSL 100MHz/200MHz LVDS Ḥ
24	NC	NC	
25	NC	NC	ΓΛ
26	NC	NC	
27	VDDO	Power	OUT3 OUT5~11/OUT3B OUT5B~11B 1.80V
28	OUT3B	Output	Output Clock3 ḭ ₣ 100MHz LP-HCSL Ḥ
29	OUT3	Output	Output Clock3 ₣ 100MHz LP-HCSL Ḥ
30	VDD_Core	Power	VCO ㄱ ㄴ 1.80V
31	VDD	Power	1.80V
32	NC	NC	
33	NC	NC	
34	OUT2B	Output	Output Clock2 ḭ ₣ 100MHz LVCMOS 100MHz LP-HCSL 200MHz LVDS Ḥ 156.25MHz LP-HCSL Ḥ
35	OUT2	Output	Output Clock2 ₣ 100MHz LVCMOS 100MHz LP-HCSL 200MHz LVDS Ḥ 156.25MHz LP-HCSL Ḥ
36	VDDO2	Power	OUT2/OUT2B PLL ㄴ 3.30V
37	OUT1B	Output	Output Clock1 ḭ ₣ 33.33MHz LVCMOS ㅋ □ β ₣ 100MHz LP-HCSL 25MHz LP-HCSL № Ḥ
38	OUT1	Output	Output Clock1 ₣ 33.33MHz LVCMOS 100MHz LP-HCSL 25MHz LP-HCSL Ḥ
39	VDDO1	Power	OUT1/OUT1B OSC 3.30V
40	TEST_OUT	Output	Ḥ o β
41	OUT11	Output	Output Clock11 ₣ 100MHz LP-HCSL Ḥ
42	OUT11B	Output	Output Clock11 ḭ ₣ 100MHz LP-HCSL Ḥ
43	VDDO	Power	OUT3 OUT5~11/OUT3B OUT5B~11B 1.80V
44	VDD	Power	1.80V
45	OUT0B	Output	Output Clock0B ₣ 25MHz/100MHz LVCMOS □ β Ḥ
46	VDDO0	Power	OUT0/OUT0B 1.80V 3.30V
47	OUT0	Output	

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LS8T41505 CPU h 7A1000 7A2000 ą

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45	OUT0B	LVCMOS	30		45	5		20	
47	OUT0	LVCMOS	20		40	10		30	
37,38	OUT1/	LVCMOS	20		30	20	24	30	
	OUT1B	LP-HCSL	13		19	31	33	37	
34,35	OUT2/	LVCMOS	20		30	20	24	30	

		LP-HCSL	13		19	31	33	37
		LVDS	70		90	10		30
28,29	OUT3/ OUT3B	LP-HCSL	13		19	31	33	37
22,23	OUT4/ OUT4B	LP-HCSL	13		19	31	33	37
		LVDS	70		90	10		30
19,20,17,18,10,11,8,9,6,7,1,48,41,42	OUT5-OUT11 /OUT5B-OUT11B	LP-HCSL	13		19	31	33	37

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4 OUT1 ڠ OUT1B OUT2 ڠ OUT2B OUT3 ڠ OUT3B OUT4 ڠ OUT4B OUT5 ڠ OUT5B OUT6 ڠ OUT6B OUT7 ڠ OUT7B OUT8 ڠ OUT8B OUT9 ڠ OUT9B OUT10 ڠ OUT10B OUT11 ڠ OUT11B ԿNo Ḥ῀

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5. ỵ Ѣ ђ Ð

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2 ỵ

⁄ VDD	0V 2.7V
ṗ ⁄ VDD_CORE	0V 2.7V
⁄ VDDA	0V 2.7V
₮ ˩ ˪ ⁄ VDDO	0V 2.7V
₮ ˩ ˪ ⁄ VDDO0	0V 5.0V
₮ ˩ ˪ ⁄ VDDO1	0V 5.0V
₮ ˩ ˪ ⁄ VDDO2	0V 5.0V
₮ ˩ ˪ ⁄ VDDO4	0V 5.0V
	-65 150
ђ	200mA
θ J_c	42 /W
ESD HBM	1000V

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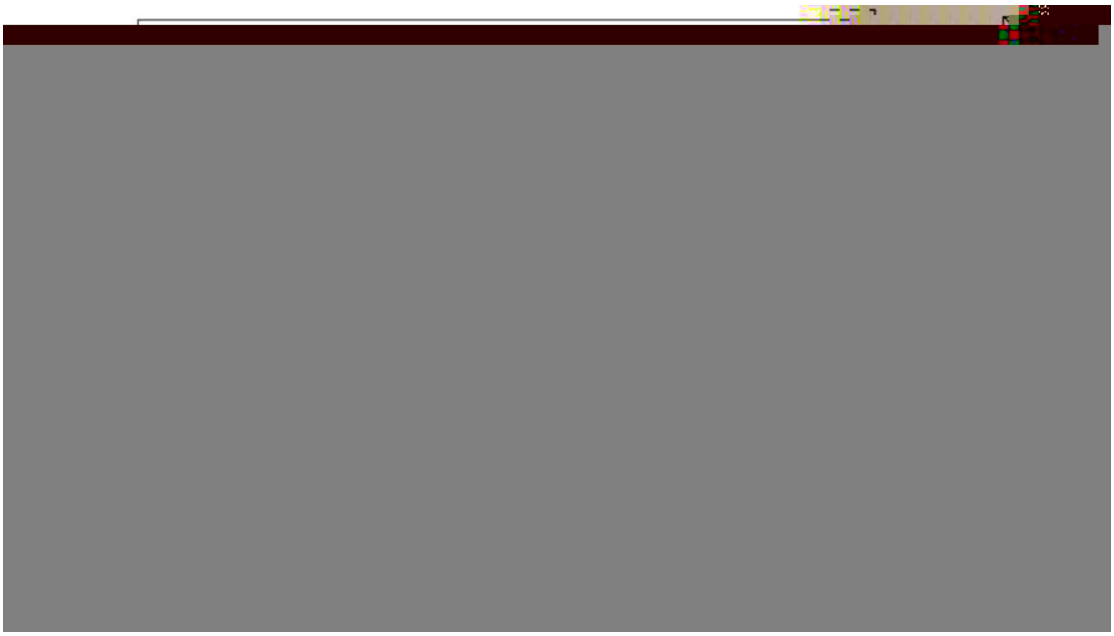
3 ђ Ð

⁄ VDD	1.8V ± 5%
ṗ ⁄ VDD_CORE	1.8V ± 5%

ㄴ VDDA	1.8V ± 5%
₮ ⌐ ㄴ ㄴ VDDO	1.8V ± 5%
₮ ⌐ ㄴ ㄴ VDDO0	1.8V ± 5%　3.3V ± 5%
₮ ⌐ ㄴ ㄴ VDDO1	3.3V ± 5%
₮ ⌐ ㄴ ㄴ VDDO2	3.3V ± 5%
₮ ⌐ ㄴ ㄴ VDDO4	3.3V ± 5%
~	25MHz ± 20ppm
ъ	-40

LVDS						
LVDS v	V_{OT}	VDD00=VDD01=VDD02=VDD04=3.3V,VD D0=VDDA=VDD_CORE=VDD=1.8V	240		460	mV
LVDS v ĩ.	ΔV_{OD}				50	mV
LVDS ˜	V_{OS}		1.12	1.3	1.40	V
LVDS ˜ ĩ.	ΔV_{OS}				50	mV
LVDS ˜	I_{OS}			12	24	mA
LVDS ˜ ĩ.	I_{OSD}			6.8	24	uA
LP-HCSL						
LPHCSL	V_{OH}	VDD00=VDD01=VDD02=VDD04=3.3V,VD D0=VDDA=VDD_CORE=VDD=1.8V	0.60		0.85	V
LPHCSL ¥	V_{OL}		-0.15		0.15	V
⁝ ˥ / Ӆ	t_R / t_F	VDD00=VDD01=VDD02=VDD04=3.3V,VD D0=VDDA=VDD_CORE=VDD=1.8V	1		3	ns
˧	t_{RF}		0.22		0.85	V/ns
~	f_{IN}			25.00		MHz
₹	f_{OUT}		25		200	MHz
VCO	f_{VCO}	VCO ƀ ॐ		2000/ 2500		MHz
☋	f_{PFD}	☋ ƀ		25		MHz
	f_{BW}	~ ч 25MHz	0.05		0.3	MHz
~ |	t_2		45		55	%
₹ |	t_3		40		60	%
˧	t_4	3.3V LVCMOS ₹ ⁝ ˥ =5pF	1.2		2.7	V/ns
⁝ ˥ / Ӆ	t_5	LVDS	0.5	1	3	ns
jitter	t_6	RMS β jitter ă OUT0 25MHz LVCMOS ₹	0.5	1	3	ps
		RMS β jitter № ₹ 100MHz LP-HCSL ₹		1	3	ps
	t_7	ɾ ⁝ ⌡ PLL		10		ms
		ɾ ą ⁝ ⌡ PLL		2	4	ms
₹ ˉ z		PCB LVCMOS			30	cm
		PCB LVDS			30	cm
		PCB LP-HCSL			30	cm



~ ǎ	MHz	ẏ KHz	ẏ KHz

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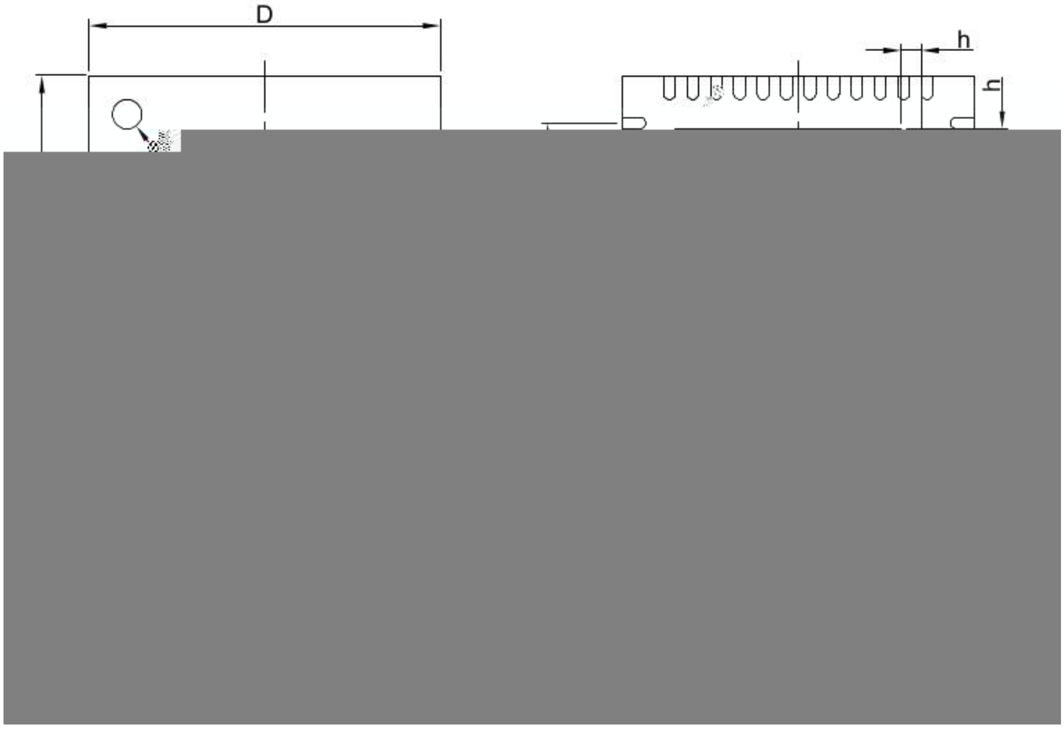

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	MIN	NOM	MAX		MIN	NOM	MAX
A	0.50	0.55	0.60	b	0.15	0.20	0.25
A1	—	0.02	0.05	c	0.12	0.15	0.18
D	5.90	6.00	6.10	h	0.30	0.35	0.40
D1	4.10	4.20	4.30	e	-	0.40	-
E	5.90	6.00	6.10	Ne	-	4.40	-
E1	4.10	4.20	4.30	Nd	-	4.40	-
L	0.35	0.40	0.45				

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10. ᪥ ج

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b ѿ ݣ Ð ﻔﻤ “ LS8T41505-A ” A ч ݣ Ð ч ݒ ʒ -i -H ч ʒ

c Ҥ B ч ≢ ╠ 4 ᵝ Ꙇ U 5 ᵝ ч ≢

d ҉ C ч ݣ Ð ↓ Ѣ ɽ 00001 Ҥ Ѣ Ҥ غ ҉

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11. Ḥ

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ﻔﻤ		ƀ
LS8T41505		0 ~+70
LS8T41505-i		-40 ~+85
LS8T41505-H		-40 ~+105

12. ą ƀ ȉ Ҥ

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كح Đ ضي

b غ كح Ǐ

c Ƅ Đ

كح Đ ضي LSD غ

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f Ḡ ضي 45%~75%

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EPAD 4.5mm SQ